

ABSTRACT OF THE DISCLOSURE

A frequency synthesizing circuit is provided. The frequency synthesizing circuit includes a frequency multiplying circuit and a phase-locked loop, wherein the frequency multiplying circuit can convert a reference signal having a low frequency into a high
5 frequency signal for being a reference signal of the phase-locked loop, so that the loop bandwidth of the phase-locked loop can be increased to reduce jitter of the output signal. The present invention utilizes the delay-locked loop to generate multiphase output signals that equivalently divide a cycle of the reference signal for achieving a frequency multiplying through cooperating with a phase synthesizer. Through double frequency
10 multiplying functions of the delay loop and the phase locked loop, a phase error accumulation caused by the single frequency multiplying of the conventional phase-locked loop with narrow loop bandwidth can be reduced. Furthermore, the frequency multiplying can be adjusted by synthesizing different phases of delay-locked loop and the divider coefficient of the phase-locked loop.